THE INVENTION CLAIMED IS:

1. An integrated circuit comprising:

a semiconductor substrate having a semiconductor device provided thereon;

a dielectric layer formed over the semiconductor substrate having an opening provided therein;

a conductor core material filling the opening and connected to the semiconductor device;

a low solubility metal-conductor interconnect cap disposed over the conductor core; and

a capping layer over the dielectric layer and the low solubility metal-conductor interconnect cap.

2. The integrated circuit as claimed in claim 1 wherein the low solubility metal-conductor interconnect cap uses a low solubility metal having a low solid solubility in the conductor core material to form an intermetallic compound therewith.

3. The integrated circuit as claimed in claim 1 wherein the low solubility metal forms an additional capping layer with the capping layer.

4. The integrated circuit as claimed in claim 1 wherein the low solubility metal-conductor interconnect cap uses a low solubility metal selected from a group consisting of cerium, lanthanum, zirconium, an alloy thereof, and a compound thereof.

5. The integrated circuit as claimed in claim 1 wherein the conductor core is a material selected from a group consisting of copper, aluminum, gold, silver, an alloy thereof, and a combination thereof.

6. An integrated circuit comprising:

a silicon substrate having a semiconductor device provided thereon;

a device dielectric layer formed over the silicon substrate;

a channel dielectric layer formed over the device oxide layer having a channel opening provided therein;

a barrier layer lining the channel opening;

a seed layer lining the barrier layer;

a conductor core filling the channel opening and connected to the semiconductor device, the conductor core over the seed layer;

a low solubility metal-conductor interconnect cap disposed over the conductor core and the seed layer; and

a capping layer over the dielectric layer and the low solubility metal-conductor interconnect cap.

7. The integrated circuit as claimed in claim 1 wherein the low solubility metal-conductor interconnect cap uses a low solubility metal having a low solid solubility in the seed layer and conductor core material to form an intermetallic compound therewith.

8. The integrated circuit as claimed in claim 1 wherein the low solubility metal forms an additional capping layer with the capping layer.

9. The integrated circuit as claimed in claim 1 wherein the low solubility metal-conductor interconnect cap uses a low solubility metal selected from a group consisting of cerium, lanthanum, zirconium, an alloy thereof, and a compound thereof.

10. The integrated circuit as claimed in claim 1 wherein the conductor core contains a material selected from a group consisting of copper, aluminum, gold, silver, an alloy thereof, and a combination thereof.

11. A method of manufacturing an integrated circuit comprising the steps of:

providing a semiconductor substrate having a semiconductor device provided thereon;

forming a dielectric layer on the semiconductor substrate;

forming an opening in the dielectric layer;

depositing a conductor core to fill the opening and connect to the semiconductor device;

planarization of the conductor core and the dielectric layer;

providing a low solubility metal oxide on the conductor core and the dielectric layer;

thermally treating of the low solubility metal oxide to cause alloying of the low solubility metal with the conductor in the conductor core to form a low solubility metal-conductor interconnect cap over the conductor core; and

forming a capping layer over the low solubility metal-conductor interconnect cap and the dielectric layer.

12. The method of manufacturing an integrated circuit as claimed in claim 11 wherein thermally treating is performed from about 150°C to about 450°C.

13. The method of manufacturing an integrated circuit as claimed in claim 11 including reduction treating the low solubility metal oxide after providing the low solubility metal oxide.

14. The method of manufacturing an integrated circuit as claimed in claim 11 wherein providing the low solubility metal oxide provides a stable oxide of a low solubility metal having a low solid solubility in the conductor core material to form an intermetallic compound therewith.

15. The method of manufacturing an integrated circuit as claimed in claim 11 wherein providing the low solubility metal oxide provides a low solubility metal selected from a group consisting of cerium, lanthanum, zirconium, a compound thereof, and a combination thereof.

16. The method of manufacturing an integrated circuit as claimed in claim 11 wherein depositing the conductor core deposits a material selected from a group consisting of copper, aluminum, gold, silver, an alloy thereof, and a compound thereof.

17. A method of manufacturing an integrated circuit comprising the steps of:

providing a semiconductor substrate having a semiconductor device provided thereon;

forming a device dielectric layer over the semiconductor substrate;

forming a channel dielectric layer over the device dielectric layer;

forming a channel opening in the channel dielectric layer layer;

depositing a barrier layer to line the channel opening;

depositing a seed layer to line the barrier layer;

depositing a conductor core to fill the channel opening and connect to the semiconductor device;

chemical-mechanical polishing of the conductor core, the seed layer, the barrier layer, and the dielectric layer;

providing a low solubility metal oxide on the conductor core, the seed layer, the barrier layer, and the dielectric layer;

thermally treating of the low solubility metal oxide to cause alloying of the low solubility metal with the conductor in the conductor core to form a low solubility metal-conductor interconnect cap over the conductor core; and

forming a capping layer over the dielectric layer and the low solubility metal-conductor interconnect cap.

18. The method of manufacturing an integrated circuit as claimed in claim 17 wherein thermally treating the low solubility metal oxide is performed from about 150°C to about 450°C for up to three hours followed by a cooling treatment.

19. The method of manufacturing an integrated circuit as claimed in claim 17 including reduction treating the low solubility metal oxide after providing the low solubility metal oxide using a reducing plasma.

20. The method of manufacturing an integrated circuit as claimed in claim 17 wherein providing the low solubility metal oxide provides a stable oxide of a low solubility metal having a low solid solubility in the conductor core material to form an intermetallic compound therewith.

21. The method of manufacturing an integrated circuit as claimed in claim 17 wherein providing the low solubility metal oxide provides a low solubility metal selected from a group consisting of cerium, lanthanum, zirconium, a compound thereof, and a combination thereof.

22. The method of manufacturing an integrated circuit as claimed in claim 17 wherein depositing the conductor core deposits a material selected from a group consisting of copper, aluminum, gold, silver, an alloy thereof, and a compound thereof.